(FILE 'USPAT' ENTERED AT 15:33:12 ON 27 JUL 1999)

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L1            30 S SIMD VECTOR
L2          2312 S PRECISION (P) EXTENDED
L3             2 S L1 AND L2
L4            65 S L2 (P) REGISTER (P) ACCUMULAT?
L5            27 S EHLIG?/IN
L6            47 S L4 NOT L5
L7             7 S GOMOLA?/IN
L8            43 S L6 NOT L7
L9            32 S INTRATER?/IN
L10           35 S L8 NOT L9
=> d 1-
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1. 5,909,572, Jun. 1, 1999, System and method for conditionally moving an operand from a source register to a destination register; John S. Thayer, et al., 712/226 [IMAGE AVAILABLE]

2. 5,900,025, May 4, 1999, Processor having a hierarchical control register file and methods for operating the same; Donald L. Sollars, 712/248 [IMAGE AVAILABLE]

3. 5,893,145, Apr. 6, 1999, System and method for routing operands within partitions of a source register to partitions within a destination register; John S. Thayer, et al., 711/125; 345/302; 708/401; 710/116; 711/146 [IMAGE AVAILABLE]

4. 5,878,266, Mar. 2, 1999, Reservation station for a floating point processing unit; Michael D. Goddard, et al., 712/23 [IMAGE AVAILABLE]

5. 5,864,703, Jan. 26, 1999, Method for providing extended precision in SIMD vector arithmetic operations; Timothy van Hook, et al., 712/22; 364/736.01; 395/562; 712/221 [IMAGE AVAILABLE]

6. 5,862,063, Jan. 19, 1999, Enhanced wavetable processing technique on a vector processor having operand routing and slot selectable operations; Gary W. Thome, et al., 364/723, 724.011, 724.1 [IMAGE AVAILABLE]

7. 5,850,227, Dec. 15, 1998, Bit map stretching using operand routing and operation selective multimedia extension unit; Brian E. Longhenry, et al., 345/439, 523; 708/290 [IMAGE AVAILABLE]

8. 5,801,975, Sep. 1, 1998, Computer modified to perform inverse discrete cosine transform operations on a one-dimensional matrix of numbers within a minimal number of instruction cycles; John S. Thayer, et al., 708/402 [IMAGE AVAILABLE]

9. 5,761,105, Jun. 2, 1998, Reservation station including addressable constant store for a floating point processing unit; Michael D. Goddard, et al., 708/510, 490; 712/222 [IMAGE AVAILABLE]

10. 5,625,828, Apr. 29, 1997, Parallel operating CPU core and DSP module for executing sequence of vector DSP code instructions to generate decoded constellation points in QAM/TCM modem application; Iddo Carmon, et al., 375/261; 364/919.4, 927.8, 927.92, 929, 931.4, 932.8, 942.8, 946.2, DIG.2; 375/265, 272 [IMAGE AVAILABLE]

11. 5,519,879, May 21, 1996, Integrated circuit having CPU and DSP for executing vector lattice propagation instruction and updating values of

vector Z in a single instruction cycle; Iddo Carmon, 712/35; 364/229, 229.2, 948.3, 948.32, DIG.1, DIG.2; 708/318 [IMAGE AVAILABLE]

12. 5,487,173, Jan. 23, 1996, DTMF detection in an integrated data processing system; Israel Greiss, et al., 712/35; 364/229.2, 232.8, 232.9, DIG.1, DIG.2; 710/5; 712/36, 227 [IMAGE AVAILABLE]

13. 5,181,226, Jan. 19, 1993, Threshold level generator; Robert H. Cantwell, 375/200; 327/97; 380/34 [IMAGE AVAILABLE]

14. 5,120,997, Jun. 9, 1992, Spread spection signal detector; Robert H. Cantwell, 327/79, 50; 375/208 [IMAGE AVAILABLE]

15. 4,972,430, Nov. 20, 1990, Spread spectrum signal detector; Robert H. Cantwell, 375/200; 380/34 [IMAGE AVAILABLE]

16. 4,876,660, Oct. 24, 1989, Fixed-point multiplier-accumulator architecture; Robert E. Owen, et al., 708/603 [IMAGE AVAILABLE]

17. 4,823,260, Apr. 18, 1989, Mixed-precision floating point operations from a single instruction opcode; Michael T. Imel, et al., 712/222; 364/223, 224, 243, 243.4, 243.41, 244, 244.3, 244.6, 247, 247.8, 256.3, 256.4, 258, 261.6, 262.4, 262.7, 262.8, DIG.1; 708/551 [IMAGE AVAILABLE]

18. 4,777,613, Oct. 11, 1988, Floating point numeric data processor; Van B. Shahan, et al., 708/510; 364/223, 224, 228.6, 240, 240.2, 240.7, 244, 244.9, 258, 258.4, 262.4, 262.8, DIG.1 [IMAGE AVAILABLE]

19. 4,680,701, Jul. 14, 1987, Asynchronous high speed processor having high speed memories with domino circuits contained therein; Michael J. Cochran, 712/40; 364/232.8, 236.2, 237.2, 237.3, 238, 243, 243.6, 246.13, 246.3, 258, 270, 270.4, 270.5, 270.9, 271.5, 281.3, DIG.1; 365/194, 233 [IMAGE AVAILABLE]

20. 4,665,500, May 12, 1987, Multiply and divide unit for a high speed processor; Sid Poland, 708/628, 656 [IMAGE AVAILABLE]

21. 4,654,786, Mar. 31, 1987, Data processor using picosquencer to control execution of multi-instruction subroutines in a single fetch cycle; Michael J. Cochran, et al., 712/242; 364/231.4, 231.6, 231.8, 238, 240, 240.2, 242.6, 242.7, 243, 243.1, 244, 244.6, 247, 247.2, 247.3, 247.4, 247.7, 261.3, 261.5, 261.6, 261.7, 262.4, 262.8, 262.9, 263, 263.1, 263.2, 280, 280.8, 281.3, DIG.1; 712/245 [IMAGE AVAILABLE]

22. 4,525,780, Jun. 25, 1985, Data processing system having a memory using object-based information and a protection scheme for determining access rights to such information; Richard G. Bratt, et al., 711/163; 364/228.3, 231.4, 231.6, 243, 244, 244.3, 246.6, 262.4, 262.8, 263, 286, 286.4, 286.5, DIG.1 [IMAGE AVAILABLE]

23. 4,507,740, Mar. 26, 1985, Programmable signal analyzer; Albert A. Star, et al., 702/57; 324/76.12, 76.15, 76.24 [IMAGE AVAILABLE]

24. 4,493,027, Jan. 8, 1985, Method of performing a call operation in a digital data processing system having microcode call and return operations; Lawrence H. Katz, et al., 712/228; 364/228.2, 228.5, 241.2, 244, 244.3, 247, 247.7, 256.3, 258, 260, 260.1, 261.3, 262.4, 262.7, 262.8, 270.5, 280.4, DIG.1; 712/243, 245 [IMAGE AVAILABLE]

25. 4,455,602, Jun. 19, 1984, Digital data processing system having an I/O means using unique address providing and access priority control techniques; Ward Baxter, III, et al., 710/5; 364/228.1, 228.3, 231.4, 231.6, 232.1, 243, 243.3, 244, 244.3, 246.6, 262.4, 262.8, 263, 280, 280.4, 281.3, 281.4, DIG.1; 710/39, 65 [IMAGE AVAILABLE]

26. 4,434,459, Feb. 28, 1984, Data processing system having instruction responsive apparatus for both a basic and an extended instruction set; Charles J. Holland, et al., 712/210; 364/232.7, 236, 236.2, 238.4, 243, 243.1, 243.4, 243.41, 244, 244.3, 244.6, 246, 246.5, 247, 247.1, 247.7, 248.1, 252, 254.9, 256.3, 258, 258.2, 259, 259.7, 259.9, 261.3, 262.4, 262.7, 262.8, 262.9, 263, DIG.1 [IMAGE AVAILABLE]

27. 4,398,243, Aug. 9, 1983, Data processing system having a unique instruction processor system; Kenneth D. Holberger, et al., 712/211; 364/228.5, 231, 231.8, 232.3, 232.7, 232.9, 236, 236.2, 238, 238.4, 239, 239.4, 239.6, 240.1, 241.2, 241.5, 242.3, 243, 243.4, 243.41, 243.6, 244, 244.3, 244.6, 244.7, 245.5, 245.8, 246, 246.1, 246.6, 246.8, 247, 247.1, 247.2, 247.3, 247.4, 247.5, 247.6, 247.7, 247.8, 251, 251.3, 252, 252.3, 252.6, 253, 253.1, 254, 254.3, 254.5, 254.6, 254.8, 254.9, 255.1, 255.2, 255.5, 256.3, 256.4, 256.5, 258, 259, 259.2, 262.4, 262.5, 262.7, 262.8, 263.1, 265, 265.2, 266.3, 266.5, 267, 267.3, 267.7, 270, 270.1, 271.6, 271.8, 285, 285.4, DIG.1 [IMAGE AVAILABLE]

28. 4,386,399, May 31, 1983, Data processing system; Edward Rasala, et al., 710/126; 364/228.5, 232.7, 232.8, 236, 236.2, 238.4, 243, 243.1, 243.4, 243.41, 243.42, 243.44, 244, 244.3, 244.6, 246, 246.5, 246.6, 246.9, 246.91, 247, 247.1, 247.7, 248.1, 256.3, 256.6, 262.4, 262.7, 262.8, 263, DIG.1; 711/1, 5, 117, 131, 158, 202 [IMAGE AVAILABLE]

29. 4,316,259, Feb. 16, 1982, Programmable function generator; Charles D. Albrecht, et al., 708/270; 714/740, 744 [IMAGE AVAILABLE]

30. 4,300,207, Nov. 10, 1981, Multiple matrix switching system; Donald J. Eivers, et al., 710/131; 324/73.1; 364/921.8, 925, 925.1, 926.9, 927.8, 927.92, 927.96, 929.1, 929.4, 933.1, 933.2, 933.6, 934, 934.2, 935, 935.2, 935.3, 935.4, 937, 938, 938.1, 938.3, 940, 941, 942, 949, 964, 964.1, DIG.2 [IMAGE AVAILABLE]

31. 4,216,528, Aug. 5, 1980, Digital computer implementation of a logic director or sequencer; James D. Robertson, 364/468.01, 221, 221.2, 221.4, 221.7, 221.9, 222.81, 222.82, 225, 226.8, 226.9, 228.3, 230, 230.1, 230.3, 232.3, 232.7, 232.9, 234, 235, 236, 236.1, 236.2, 236.3, 236.5, 237, 237.2, 237.4, 237.8, 241.2, 248, 248.1, 248.3, 254.9, 258, 258.1, 258.2, 258.3, 259, 259.2, 259.5, 259.7, 259.8, 260, 260.2, 260.4, 260.8, 261.3, 261.4, 261.5, 262.4, 262.5, 264, 264.6, 271, 271.5, 280, 280.2, 281.3, 281.8, DIG.1; 709/101 [IMAGE AVAILABLE]

32. 3,835,260, Sep. 10, 1974, COMMUNICATION SWITCHING SYSTEM, WITH MARKER, REGISTER, AND OTHER SUBSYSTEMS COORDINATED BY A STORED PROGRAM CENTRAL PROCESSOR; Kenneth E. Prescher, et al., 379/237, 269, 273, 279, 290, 302 [IMAGE AVAILABLE]

33. 3,786,436, Jan. 15, 1974, MEMORY EXPANSION ARRANGEMENT IN A CENTRAL PROCESSOR; Paul Z. Zelinski, et al., 711/213; 364/222.2, 222.3, 228.1, 228.3, 228.5, 236, 236.3, 236.4, 238, 238.2, 238.4, 240.1, 241.2, 241.5, 244, 244.6, 245, 245.1, 245.4, 246, 246.3, 246.6, 246.8, 248, 248.3, 251,

251.1, 252, 254, 254.3, 254.4, 255.1, 255.2, 255.8, 260, 260.2, 261, 261.2, 261.3, 261.4, 261.5, 261.6, 265, 265.6, 266.4, 266.5, 267, 267.2, 267.4, 268, 268.1, 270, 270.1, 271, 271.2, 271.5, 271.6, 271.8, DIG.1 [IMAGE AVAILABLE]

34. 3,761,893, Sep. 25, 1973, DIGITAL COMPUTER; Richard E. Morley, 711/151; 364/221.9, 222, 222.2, 223, 232.9, 240.1, 242.1, 242.4, 243, 243.5, 244, 244.6, 246, 246.1, 248, 248.2, 248.3, 254.8, 259, 259.1, 259.5, 260, 262.4, 262.8, DIG.1; 711/107 [IMAGE AVAILABLE]

35. 3,740,722, Jun. 19, 1973, DIGITAL COMPUTER; Michael P. Greenberg, et al., 710/269; 364/229, 229.2, 230, 230.3, 232.9, 239, 239.4, 240.1, 242.4, 243, 243.2, 245, 245.2, 245.5, 245.6, 246, 246.2, 246.6, 254.8, 256.8, 270, 271.6, DIG.1 [IMAGE AVAILABLE]
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